High Performance, Constant Current LED Driver with PWM Brightness Control

Features

- 4.5V to 65V Input Voltage
- 2Ω, 1A Peak MOSFET Gate Drive
- Differential, High-Side Current Sense
- Cycle-by-Cycle Current Limit
- 10,000:1 PWM Dimming Range
- 250:1 Analog Dimming Range
- Supports All-Ceramic Output Capacitors and Capacitor-less Outputs
- Low-Power Shutdown and Thermal Shutdown
- No Control Loop Compensation Required
- Thermally Enhanced 10-Pin, SSOP10 Package

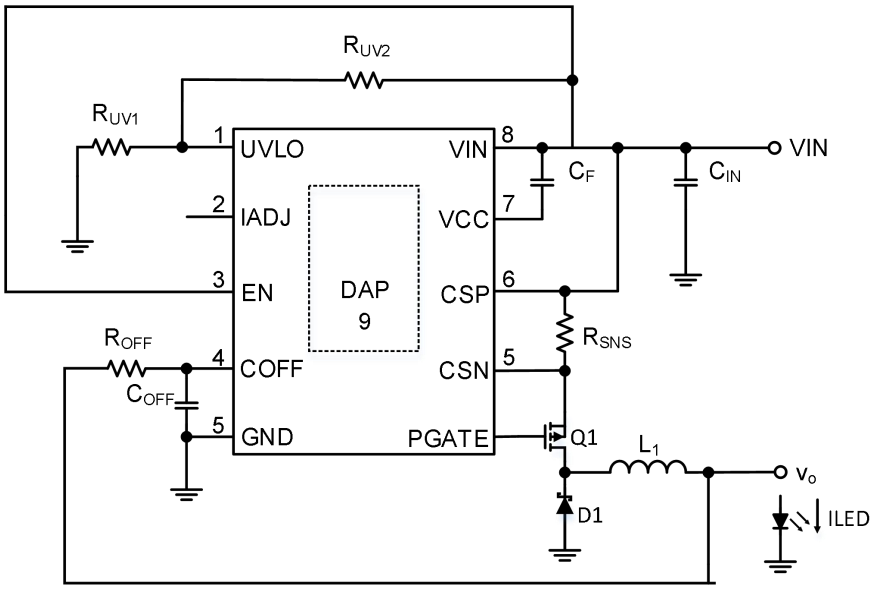
Applications

- LED Driver
- Automotive Lighting
- Constant Current Source
- General Illumination

General Description

The 3409 are P-channel MOSFET (PFET) controllers for step-down (buck) current regulators. They offer wide input voltage range, high-side differential current sense with low adjustable threshold voltage and fast output enable/disable function and a thermally enhanced 10-pin, SSOP10 package. It accepts input voltages from 4.5V to 65V and deliver up to 1A average LED current with ±3% accuracy. The3409 devices use constant off-time (COFT) control to regulate an accurate constant current without the need for external control loop compensation. Analog and PWM dimming are easy to implement and result in a highly linear dimming range with excellent achievable contrast ratios. Programmable UVLO, low-power shutdown, and thermal shutdown complete the feature set.

Typical Application Circuit



Typical Application Circuit

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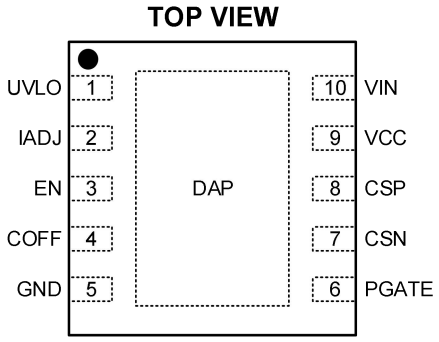
Package and Pin Description

Pin Configuration



Top Marking: JGYLL (device code: JG, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	UVLO	Input undervoltage lockout. Connect to a resistor divider from VIN and GND. Turn-on threshold is 1.24V and hysteresis for turnoff is provided by a 22μA current source.
2	IADJ	Analog LED current adjust. Apply a voltage from 0 to 1.24V, connect a resistor to GND, or leave open to set the current sense threshold voltage.
3	EN	Logic level enable and PWM dimming. Apply a voltage >1.74V to enable device, a PWM signal to dim, or a voltage <0.5V for low-power shutdown.
4	COFF	Off-time programming. Connect resistor from VO, capacitor to GND to set off-time.
5	GND	Connect to system ground.
6	PGATE	Gate drive. Connect to gate of external P-channel MOSFET.
7	CSN	Negative current sense. Connect to negative side of sense resistor.
8	CSP	Positive current sense. Connect to positive side of sense resistor (also to VIN).
9	VCC	VIN– referenced linear regulator output. Connect at least a 1μF ceramic capacitor to VIN. The regulator provides power for the P-channel MOSFET drive.
10	VIN	Input voltage. Connect to the input voltage.
---	Thermal pad	Connect to GND pin.

Order Information (1)

Marking	Part No.	Model	Description	Package	T/R Qty
JGYLL	70380060	LZ3409	LZ3409 Dimmable BUCK LED Driver, V_{IN} 4.5-65V, SSOP10	SSOP10	3000PCS

Note (1): All CHIP parts are Pb-Free and adhere to the RoHS directive.

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Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
$V_{IN,}$ EN, UVLO to GND	-0.3	65	V
V_{IN} to VCC, PGATE	-0.3	7	V
V_{IN} to CSP, CSN	–0.3	0.3	V
COFF to GND	–0.3	4	V
COFF Current		±1	mA
IADJ Current		±5	mA
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\ (MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	4.5	65	V
Output Current	0	1	A

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature

limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	54.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.
Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1) (2)

V_{IN}=24V, T_A=25°C, unless otherwise specified.

Parameter		Test Conditions	Min	Typ.	Max	Unit
Peak Current Comparator						
V_{CST}	V_{CSP}-V_{CSN} Average Peak Current Threshold	V_{ADJ} = 1V	188	198	208	mV
		V_{ADJ} = V_{ADJ-OC}	231	246	261	
A_{ADJ}	V_{ADJ} to V_{CSP}-VCSN threshold gain	0.1 < V_{ADJ} < 1.2V V_{ADJ} = V_{ADJ-OC}		0.2		V/V
V_{ADJ-OC}	I_{ADJ} Pin Open Circuit Voltage		1.189	1.243	1.297	V
I_{ADJ}	I_{ADJ} Pin Current		3.8	5	6.4	μA
T_{DEL}	CSN Pin Falling Delay	CSN Fall-PGATE Rise		38		ns
System Currents						
I_{IN}	Operating Input Current	Not Switching		2		mA
I_{SD}	Shutdown Input Current	EN = 0V		110		μA
PFET Diver						
R_{PGATE}	Driver Output Resistance	Sourcing 50mA		2		Ω
		Sinking 50mA		2		
VCC Regulator						
V_{CC}	V_{IN} Pin Voltage-V_{CC} Pin Voltage	V_{IN} > 9V 0 <ICC< 20mA	5.5	6	6.5	V
$V_{CC-UVLO}$	V_{CC} Undervoltage Lockout Threshold	V_{CC} Increasing		3.73		V
V_{CC-HYS}	V_{CC} UVLO Hysteresis	V_{CC} Decreasing		283		mV
I_{CC-LIM}	V_{CC} Regulator Current Limit		30	45		mA
OFF-Timer and ON-Timer						

V_{OFT}	Off-Time Threshold		1.122	1.243	1.346	V
t_{D-OFF}	COFF Threshold to PGATE Falling Delay			25		ns
t_{ON-MIN}	Minimum On-Time			115	211	ns
$t_{OFF-MAX}$	Maximum Off-Time			300		µs
Undervoltage Lockout						
I_{UVLO}	UVLO Pin Current	V_{UVLO} = 1V		10		nA
V_{UVLO-R}	Rising UVLO Threshold		1.175	1.243	1.311	V
$I_{UVLO-HYS}$	UVLO Hysteresis Current			22		µA
Enable						
I_{EN}	EN Pin Current			10		nA
V_{EN-TH}	EN Pin Threshold	V_{EN} Rising			1.74	V
		V_{EN} Falling	0.5			
V_{EN-HYS}	EN Pin Hysteresis			420		mV
t_{EN-R}	EN Pin Rising Delay	EN Rise-PGATE Fall		42		ns
t_{EN-F}	EN Pin Falling Delay	EN Fall-PGATE Rise		21		ns

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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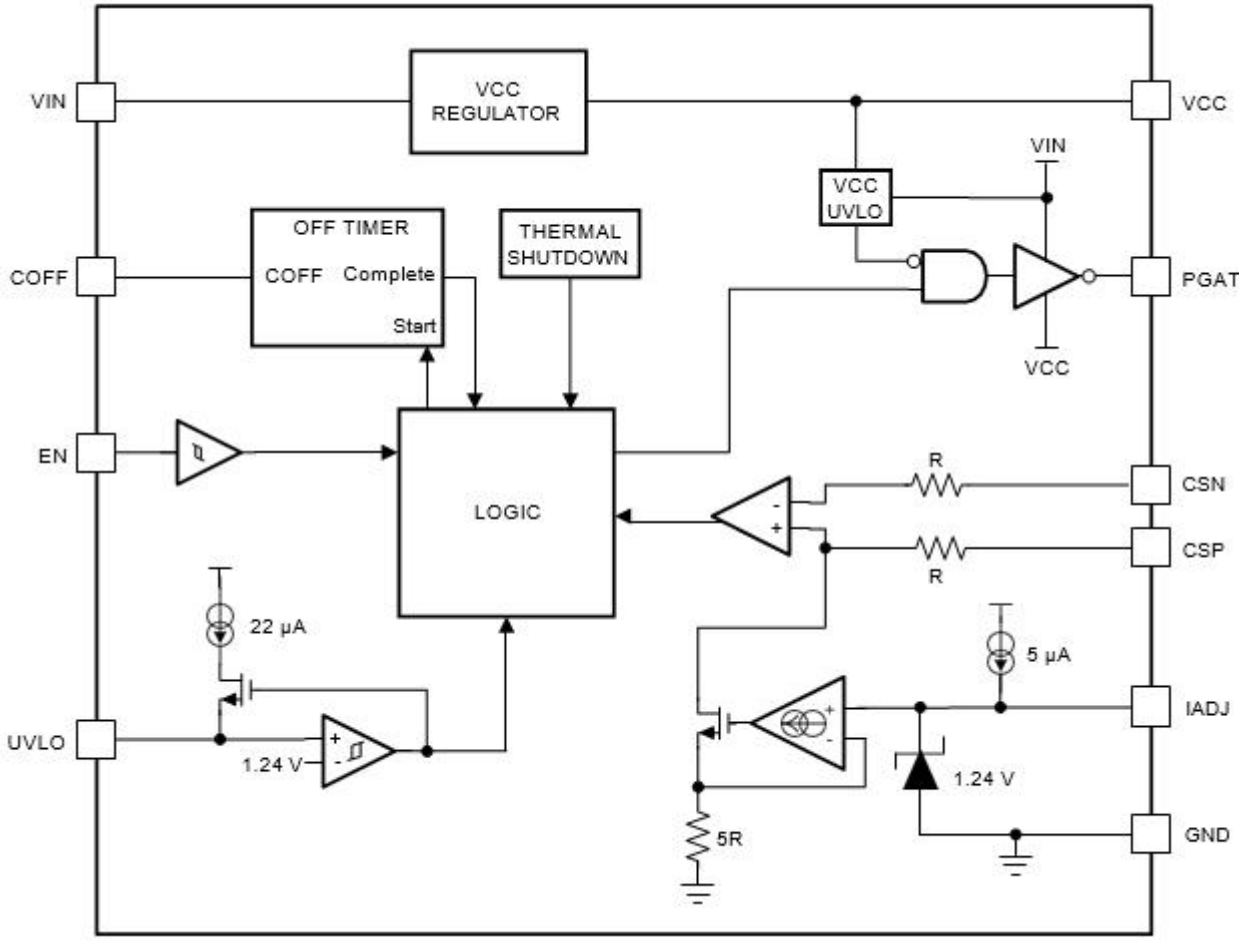
Functional Block Diagram



Block Diagram

Functions Description

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Enable and PWM Dimming

The enable pin (EN) is a compatible input for PWM dimming of the LED. A logic low (below 0.5V) at EN will disable the internal driver and shut off the current flow to the LED array. While the EN pin is in a logic low state the support circuitry (driver, bandgap, VCC regulator) remains active to minimize the time needed to turn the LED array back on when the EN pin sees a logic high (above 1.74 V). The LED current rise and fall times (which are limited by the slew rate of the inductor as well as the delay from activation of the EN pin to the response of the external PFET) limit the achievable T_{DIM} and D_{DIM}. In general, dimming frequency should be at least one order of magnitude lower than the steady state switching frequency to prevent aliasing. However, for good linear response

across the entire dimming range, the dimming frequency may need to be even lower.

Controlled Off-Time (COFT) Architecture

The COFT architecture is used by the 3409 to control I_{LED}. It is a combination of peak current detection and a one-shot off-timer that varies with output voltage. For any buck regulator, D is simply the conversion ratio divided by the efficiency (η):

$$D = \frac{V_O}{\eta \times V_{IN}}$$

D is indirectly controlled by changes in both t_{OFF} and t_{ON}, which vary depending on the operating point. This creates a variable switching frequency over the entire operating range. This type of hysteretic control eliminates the need for control loop compensation necessary in many switching regulators, simplifying the design process and providing fast transient response.

Peak Switch Current Limit

At the beginning of a switching period, PFET is turned on and inductor current increases. Once peak current is detected, PFET turned off, the diode forward biases, and inductor current decreases. Peak current detection accomplished with using the differential voltage signal created as current flows through the current setting resistor (R_{SNS}). The voltage across R_{SNS} (V_{SNS}) is compared to the adjustable current sense threshold (V_{CST}) and PFET is turned off when VS_{NS} exceeds V_{CST}, providing that t_{ON} is greater than the minimum possible t_{ON} (typically 115ns).

Output Overvoltage protection

Because the LZ3409 controls a buck current regulator, there is no inherent need to provide output overvoltage protection. If the LED load is opened, the output voltage will only rise as high as the input voltage plus any ringing due to the parasitic inductance and capacitance present at the output node. If a ceramic output capacitor is used in the application, it should have a minimum rating equal to the input voltage. Ringing seen at the output node should not damage most ceramic capacitors, due to their high ripple current rating.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Applications Information

Setting the LED Current

The 3409 requires no external current sensing resistor for LED current regulation. The average output current of the 3409 is adjustable by varying the resistance of the resistor, R_{IADJ} that connects across the IADJ and GND pins. The IADJ pin is internally biased to 1.255V. The LED current is then governed by following Equation: $I_{LED} = \frac{3125\times10^3}{R_{IADJ}}$ mA, Where 350mA<I_{LED}<1A.

I_{LED} (mA)	R_I (KΩ)
350	8.93
500	6.25
700	4.46
1000	3.13

The LED current can be set to any level in the range from 350 mA to 1A. When the overcurrent protection is activated, current regulation cannot be maintained until the overcurrent condition is cleared.

Setting the Switch Frequency

The switching frequency is dependent upon the actual operating point (V_{IN} and V_O). V_O will remain relatively constant for a given application. Therefore, the switching frequency will vary with V_{IN} (frequency increases as V_{IN} increases). The target switching frequency (f_{SW}) at the nominal operating point is selected based on the tradeoffs between efficiency (better at low frequency) and solution size/cost (smaller at high frequency). The off-time of the 3409 can be programmed for switching frequencies up to 5 MHz (theoretical limit imposed by minimum t_{ON}). In practice, switching frequencies higher than 1MHz may be difficult to obtain due to gate drive limitations, high input voltage, and thermal considerations. At CCM operating points, f_{SW} is defined as:

$$f_{SW} = \frac{1-D}{t_{OFF}} = \frac{1-\left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}}$$

At DCM operating points, f_{SW} is defined as:

$$f_{SW} = \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{\left(\frac{I_{L-MAX}\times L_1}{V_{IN}-V_O}\right)+t_{OFF}}$$

Calculate the value of R_{FS} for 500-kHz switching frequency using a standard value of RFS = 40.2k Ω .

Inductor Selection

To ensure proper output current regulation, the 3409 must operate in Continuous Conduction Mode (CCM). With the incorporation of PLM, the peak-to-peak inductor current ripple can be set as high as ±60% of the defined average output current. The minimum inductance of the inductor is decided by the defined average LED current and allowable inductor current ripple. Calculate the minimum inductor value required for 600 mA or less peak-to-peak LED current ripple using Equation:

$$L_{MIN} = \frac{(V_{IN}-V_{LED})\times V_{LED}}{f_{SW}\times V_{IN}\times \Delta i_{L-PP}}$$

Choose a higher standard value of L = 47µH.

Output Capacitor Selection

Because current is being regulated, not voltage, a buck current regulator is free of load current transients, therefore output capacitance is not needed to supply the load and maintain output voltage. This is very helpful when high frequency PWM dimming the LED load. When no output capacitor is used, the same design equations that govern $\Delta i_{L\text{-}PP}$ also apply to $\Delta i_{LED\text{-}PP}$. A capacitor placed in parallel with the LED load can be used to reduce $\Delta i_{LED\text{-}PP}$ while keeping the same average current through both the inductor and the LED array. With an output capacitor, the inductance can be lowered, making the magnetics smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces $\Delta i_{LED\text{-}PP}$ to well below the target provides headroom for changes in inductance or V_{IN} that might otherwise push the maximum $\Delta i_{LED\text{-}PP}$ too high.

Input Capacitor Selection

Input capacitors are selected using requirements for minimum capacitance and RMS ripple current. The PFET current during t_{ON} is approximately I_{LED}, therefore the input capacitors discharge the difference between I_{LED} and the average input current (I_{IN}) during t_{ON}. During t_{OFF}, the input voltage source charges up the input capacitors with I_{IN}. The minimum input capacitance ($C_{IN\text{-}MIN}$) is selected using the maximum input voltage ripple ($\Delta v_{IN\text{-}MAX}$) which can be tolerated. $\Delta v_{IN\text{-}MAX}$ is equal to the change in voltage across C_{IN} during t_{ON} when it supplies the load current. A good starting point for selection of C_{IN} is to use $\Delta v_{IN\text{-}MAX}$ of 2% to 10% of V_{IN}. $C_{IN\text{-}MIN}$ can be selected as follows:

$$C_{IN} = \frac{I_{LED} \times t_{ON}}{\Delta V_{IN-MAX}} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF}\right)}{\Delta V_{IN-MAX}}$$

An input capacitance at least 75% greater than the calculated $C_{IN\text{-}MIN}$ value is recommended. To determine the RMS input current rating ($I_{IN\text{-}RMS}$) the following approximation can be used:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1-D)} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

Because this approximation assumes there is no inductor ripple current, the value should be increased by 10-30% depending on the amount of ripple that is expected. Careful selection of the capacitor requires checking capacitance ratings at the nominal operating voltage and temperature.

Diode Selection

A re-circulating diode is required to carry the inductor current during t_{OFF}. The most efficient choice is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Like PFET, diode must have a voltage rating at least 15% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current.

Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. Input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with an enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

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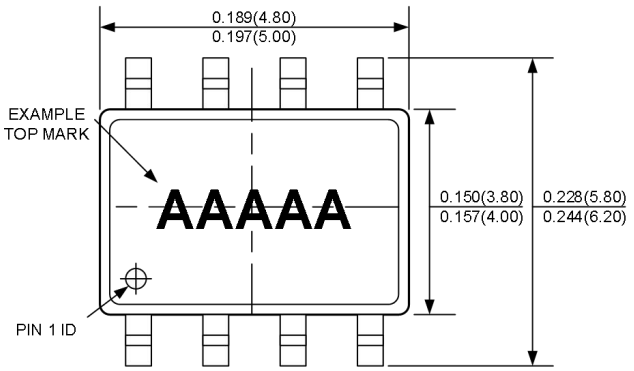
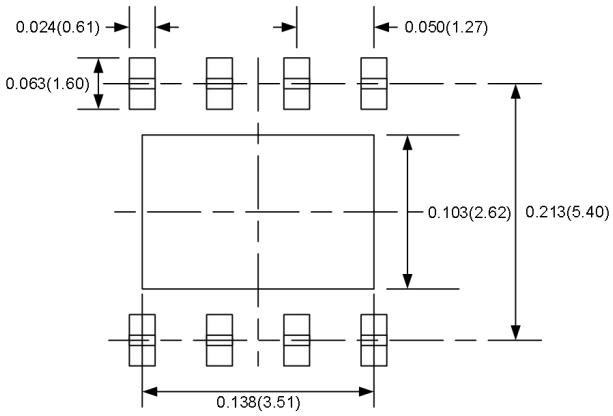
Package Description

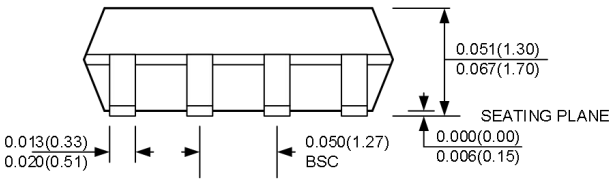
ESOP8 (EXPOSED PAD)



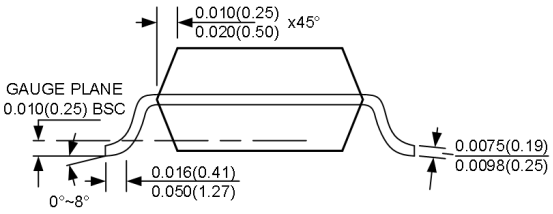
TOP VIEW



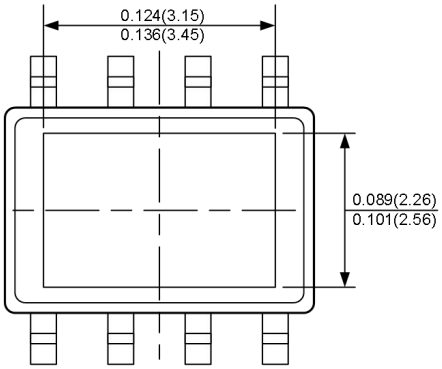
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.